A B S T R A C T

A sychronization circuit comprising an analog feedback shift register for generating an internal sequence which is synchronized with an external sequence containing repetitions of a fundamental sequence has a feedback circuit which, for the formation of a new value of a fundamental sequence, combines at least two values (x_1,x_2) stored in the shift register according to a feedback function ($f(x_1,x_2)$), which is then scaled with a factor k, $0.9<k<0.99$. The synchronization behaviour is improved, especially in the case of signals with strong background noise, by using a feedback function which is substantially linear in the sectors defined by the signs of the arguments and whose sign corresponds to that of the negative of the product of the negative arguments and whose magnitude is 1 if the magnitudes of the arguments are each 1. A function which meets these requirements and has proved useful is $f(x_1,\ldots,x_m) = -sig((-x_1)\cdot\ldots\cdot(-x_m))\cdot(|x_1|+\ldots+|x_m|)/m$. For improving the signal/noise ratio, there is a buffer in front of the analog feedback shift register, where, for the generation of the external sequence, segments of an input sequence which contain several, e.g. twenty, successive instances of the fundamental sequence are added and then read out repeatedly.

(Fig. 2)